Please amend the title to read as follows:

"METHOD OF CHECKING ALIGNMENT ACCURACY OF PATTERNS ON STACKED SEMICONDUCTOR LAYERS"

Please amend the following paragraphs of the specification in the manner indicated:

[0001] The present invention relates to a method of checking ~~overlap~~ relative alignment accuracy of patterns transferred on four stacked semiconductor layers, and more particularly to ~~forming~~ defining checking patterns on four stacked semiconductor layers and measuring ~~overlap~~ relative alignment errors thereof by the method.

[0002] Semiconductor integrated circuits with a plurality of semiconductor layers are fabricated by deposition, photolithography, etching, implantation, and thermal processes, repeatedly. In photolithography, ~~overlap~~ relative alignment accuracy of patterns transferred on semiconductor layers is critical for semiconductor device fabrication.

[0003] FIG. 1A shows a top view of a wafer 1 which is divided into several zones by scribe lines. A plurality of checking patterns are exposed inside predetermined zones 50. The checking patterns are arranged vertically to each other to measure the ~~overlap~~ relative alignment error between the patterns on adjacent semiconductor layers in two dimensions. When the checking patterns on separate semiconductor layers ~~overlap~~ align accurately, the resulting target patterns 60 align with each other accurately. FIG. 1B shows checking patterns ~~formed~~ defined by conventional photomask exposing. In FIG. 1B, a rectangular checking pattern 12 is ~~formed~~ defined on a first semiconductor layer 10 and a square checking pattern

22 is ~~formed~~ defined on a second semiconductor layer 20, wherein the rectangular checking pattern 12 lies at the center of the square checking pattern 22 and the four sides of the rectangular checking pattern 12 are parallel to the four sides of the square checking pattern 22 correspondingly. When the rectangular checking pattern 12 is located at the center of the square checking pattern 22, the target patterns on the other zones of the first semiconductor layer 10 are accurately ~~overlapped~~ aligned with the target patterns on the other zones of the second semiconductor layer 20. Furthermore, as shown in FIG. 1B, a rectangular checking pattern 12 is ~~formed~~ defined on a first semiconductor layer 10 and a square checking pattern 32 is ~~formed~~ defined on a third semiconductor layer 30, wherein the rectangular checking pattern 12 lies at the center of the square checking pattern 32 and the four sides of the rectangular checking pattern 12 are parallel to the four sides of the square checking pattern 32 correspondingly. When the rectangular checking pattern 12 is located at the center of the square checking pattern 32, target patterns on the other zones of the first semiconductor layer 10 are accurately ~~overlapped~~ aligned with target patterns on the other zones of the third semiconductor layer 30.

[0006] To solve the disadvantage mentioned above, a method of checking ~~overlap~~ relative alignment accuracy of patterns on four stacked semiconductor layers is provided according to the present invention. The target patterns on the fourth semiconductor layer formed by the method align with the target patterns on the first semiconductor layer along a

first dimension, and the target patterns on the fourth semiconductor layer also align with the target patterns on the second and third semiconductor layer along a direction perpendicular to the first dimension.

[0007] One object of the present invention is to provide a method of checking ~~overlap~~ relative alignment accuracy of patterns on a fourth semiconductor layer. The method comprises the following steps: ~~forming~~ defining a first checking pattern on a first semiconductor layer, a second checking pattern on a second semiconductor layer, a third checking pattern on a third semiconductor layer and a fourth checking pattern on a fourth semiconductor layer, wherein the first, second and third checking patterns ~~overlap~~ align to ~~form~~ define a first rectangular frame, the fourth checking pattern is surrounded by the first rectangular frame, a first pair of parallel sides of the first rectangular frame is ~~formed~~ defined by the first checking pattern, and a second pair of parallel sides of the first rectangular frame is ~~formed~~ defined by the second and third checking patterns; measuring ~~overlap~~ relative alignment accuracy between the fourth checking pattern and the first checking pattern; and measuring ~~overlap~~ relative alignment accuracy between the fourth checking pattern and the second and third checking patterns

[0008] One feature of the present invention is the definition ~~formation~~ of the first checking pattern on a first semiconductor layer, the second checking pattern on a second semiconductor layer, the third checking pattern on a third semiconductor layer and a second rectangular frame as

the fourth checking pattern on a fourth semiconductor layer, wherein the first, second and third checking patterns ~~overlap~~ align to ~~form~~ define the first rectangular frame, the fourth checking pattern is surrounded by the first rectangular frame, and the second checking pattern is parallel to the third checking pattern.

[0009] Another feature of the present invention is that two pairs of first parallel line-shaped patterns are ~~formed~~ defined on the first semiconductor layer, a pair of second parallel line-shaped patterns is ~~formed~~ defined on the second semiconductor layer, a pair of third parallel line-shaped patterns is ~~formed~~ defined on the third semiconductor layer, and a second rectangular frame as the fourth line-shaped patterns is ~~formed~~ defined on the fourth semiconductor layer. Accordingly, the first, second and third checking patterns ~~overlap~~ align to ~~form~~ define the first rectangular frame and the fourth checking pattern is surrounded by the first rectangular frame.

[0012] FIG. 1A is the top view of a wafer showing a plurality of checking patterns ~~formed~~ defined inside the scribe lines;

[0013] FIG. 1B illustrates the checking patterns ~~formed~~ defined by conventional aligner photomask;

[0014] FIG. 2A shows a first checking pattern ~~formed~~ defined on a first semiconductor layer according to the first embodiment in the present invention;

[0015] FIG. 2B shows a second checking pattern ~~formed~~ defined on a second semiconductor layer according to the first embodiment in the present invention;

[0016] FIG. 2C shows a third checking pattern ~~formed~~ defined on a third semiconductor layer according to the first embodiment in the present invention;

[0017] FIG. 2D shows a fourth checking pattern ~~formed~~ defined on a fourth semiconductor layer according to the first embodiment in the present invention;

[0018] FIG. 3A shows a first checking pattern ~~formed~~ defined on a first semiconductor layer according to the second embodiment in the present invention;

[0019] FIG. 3B shows a second checking pattern ~~formed~~ defined on a second semiconductor layer according to the second embodiment in the present invention;

[0020] FIG. 3C shows a third checking pattern ~~formed~~ defined on a third semiconductor layer according to the second embodiment in the present invention;

[0021] FIG. 3D shows a fourth checking pattern ~~formed~~ defined on a fourth semiconductor layer according to the second embodiment in the present invention;

[0027] FIG. 2A shows a first checking pattern ~~formed~~ defined on a first semiconductor layer according to the first embodiment in the present invention. In FIG. 2A, the

first checking pattern 110 comprises two pairs of first line-shaped patterns 110a and 110b parallel to each other and both the first line-shaped patterns 110a and 110b comprise two parallel lines. The first checking pattern 110 is ~~formed~~ defined by exposing a first photomask on the first semiconductor layer 100 and then developing the pattern 110 thereon.

[0028] FIG. 2B shows a second checking pattern ~~formed~~ defined on a second semiconductor layer according to the first embodiment in the present invention. In FIG. 2B, the second checking pattern comprises a pair of second parallel line-shaped patterns 220. Two lines of the second parallel line-shaped patterns 220 are parallel to each other. The second checking pattern 220 is ~~formed~~ defined by exposing a second photomask on the second semiconductor layer 200 and then developing the pattern 220 thereon.

[0029] FIG. 2C shows a third checking pattern ~~formed~~ defined on a third semiconductor layer according to the first embodiment in the present invention. In FIG. 2C, the third checking pattern comprises a pair of third parallel line-shaped patterns 330. Two lines of the third parallel line-shaped patterns 330 are parallel to each other. The third checking pattern 330 is ~~formed~~ defined by exposing a third photomask on the third semiconductor layer 300 and then developing the pattern 330 thereon.

[0030] As FIG. 2C shows, the two pairs of first line-shaped patterns 110a and 110b, the pair of second parallel line-shaped patterns 220 and the pair of third parallel line-

shaped patterns 330 are arranged to ~~form~~ define a first rectangular frame 500. The first pair of parallel sides 510 of the first rectangular frame 500 is constructed by the first line-shaped patterns 110a and 110b, and the second pair of parallel sides 520 of the first rectangular frame 500 is constructed by the second parallel line-shaped patterns 220 and the third parallel line-shaped patterns 330. The third parallel line-shaped patterns 330 are located outside the second pair of parallel sides 520 of the first rectangular frame 500 and the second parallel line-shaped patterns 220 are located inside the second pair of parallel sides 520. Accordingly, the interval between the two lines of the third parallel line-shaped patterns 330 is larger than the interval between the two lines of the second parallel line-shaped patterns 220.

[0031] FIG. 2D shows a fourth checking pattern ~~formed~~ defined on a fourth semiconductor layer according to the first embodiment in the present invention. The fourth checking pattern 440 is ~~formed~~ defined by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 2D shows, the fourth photomask defines a second rectangular frame 600 as the fourth checking pattern 440 constructed by four lines on the fourth semiconductor layer 400 and the fourth checking pattern 440 is surrounded by the first rectangular frame 500.

[0032] After the checking patterns are ~~formed~~ defined on the four stacked semiconductor layers, ~~overlap~~ alignment accuracy of the resulting target patterns on the four

semiconductor layer is measured by overlay scanning. As FIG. 2D shows, the center position of the first checking pattern 110 along the first dimension (i.e. Y-axis) is obtained and the center position of the fourth checking pattern 440 along the Y-axis is also measured. When the difference between the center position of the first checking pattern 110 along the Y-axis and the center position of the fourth checking pattern 440 along the Y-axis is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the first semiconductor layer along the Y-axis.

[0035] FIG. 3A shows a first checking pattern ~~formed~~ defined on a first semiconductor layer according to the second embodiment in the present invention. In FIG. 3A, the first checking pattern comprises a pair of first parallel line-shaped patterns with two parallel lines. The first checking pattern 110 is ~~formed~~ defined by exposing a first photomask on the first semiconductor Layer 100 and then developing the pattern 110 thereon.

[0036] FIG. 3B shows a second checking pattern ~~formed~~ defined on a second semiconductor layer according to the second embodiment in the present invention. In FIG. 3B, the second checking pattern comprises the second line-shaped pattern 220 located on one side of the first checking pattern 110 and perpendicular to the first checking pattern 110. The second checking pattern 220 is ~~formed~~ defined by exposing a second photomask on the second semiconductor layer 200 and then developing the pattern 220 thereon.

[0037] FIG. 3C shows a third checking pattern ~~formed~~ defined on a third semiconductor layer according to the second embodiment in the present invention. In FIG. 3C, the third checking pattern comprises the third line-shaped pattern 330 located on one side of the first checking pattern 110 and perpendicular to the first checking pattern 110. The third checking pattern 330 is ~~formed~~ defined by exposing a third photomask on the third semiconductor layer 300 and then developing the pattern 330 thereon.

[0038] As FIG. 3C shows, the pair of first parallel line-shaped patterns 110, the second line-shaped pattern 220 and the third line-shaped pattern 330 are arranged to ~~form~~ define a first rectangular frame 500. The first pair of parallel sides 510 of the first rectangular frame 500 is constructed by the first parallel line-shaped patterns 110, and the second pair of parallel sides 520 of the first rectangular frame 500 is constructed by the second line-shaped pattern 220 and the third line-shaped pattern 330. The third line-shaped pattern 330 is parallel to the second line-shaped pattern 220 and the second and third line-shaped patterns are on the two sides of the second pair of parallel sides 520 of the first rectangular frame 500 respectively.

[0039] FIG. 3D shows a fourth checking pattern ~~formed~~ defined on a fourth semiconductor layer according to the second embodiment in the present invention. The fourth checking pattern 440 is ~~formed~~ defined by exposing the fourth photomask on the fourth semiconductor layer 400 and

then developing the pattern 440 thereon. As FIG. 3D shows, the fourth photomask defines a second rectangular frame 600 as the fourth checking pattern 440 constructed by four lines on the fourth semiconductor layer 400 and the fourth checking pattern 440 is surrounded by the first rectangular frame 500.

[0042] FIG. 4A shows one modification of the first embodiment in the present invention. The third parallel line-shaped patterns 330 are located inside the second pair of parallel sides ~~520~~ of the first rectangular frame 500 and the second parallel line-shaped patterns 220 are located outside the second pair of parallel sides ~~520~~. Accordingly, the interval between the two lines of the second parallel line-shaped patterns 220 is larger than the interval between the two lines of the third parallel line-shaped patterns 330. The third parallel line-shaped patterns 330 are parallel to the second parallel line-shaped patterns 220.

[0043] FIG. 4B shows another modification of the first embodiment in the present invention. The fourth checking pattern 440 is ~~formed~~ defined by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 4B shows, the fourth photomask defines a second rectangular pattern as the fourth checking pattern 440 on the fourth semiconductor layer 400 and the fourth checking pattern 440 is surrounded by the first rectangular frame 500.

[0047] The ~~overlap~~ relative alignment accuracy of the target patterns on four stacked semiconductor layers is checked according to the first and second embodiments in the present invention. The ~~overlap~~ relative alignment accuracy of the target patterns on the first and the fourth semiconductor layer is measured along the first dimension and the ~~overlap~~ relative alignment accuracy of the target patterns on the second, third and fourth semiconductor layer is measured along a direction perpendicular to the first dimension.